

REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

Claims 1-16 are pending in this application, with claims 1-13 being withdrawn. Claims 14-16 have been amended. No new matter has been presented. Applicants respectfully submit that amended claims 14-16 are in condition for allowance.

In the Office Action, the drawings were objected to, a new title, more indicative of the invention, was required, claims 14-16 were rejected under 35 U.S.C. §112, first paragraph, claim 16 was rejected under 35 U.S.C. §112, second paragraph, and claims 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Tanaka et al. (U.S. 6,635,505). These grounds of objection and rejection are respectfully traversed for the following reasons.

The features of “a liquid crystal layer” and “a polysilicon semiconductor film” within Claim 14 have been deleted to comply with the requirements of 35 U.S.C. §112 and 37 C.F.R. §1.83 (a). As such, the objection to the drawings and the §112, first paragraph, rejection are believed to be overcome.

Further, the subject matter of Claims 14-16 is now more consistent with the original title of the application. Consequently, a new title is no longer believed to be required.

Also, the language of Claim 16 has been amended to recite “wherein said first and second gate dielectric layers...” to provide appropriate antecedent basis.

In addition, Claim 14 has also been amended to add a feature of “a second gate dielectric layer formed on said substrate covering said second channel and said second source/drain

regions". This feature is fully supported by the original specification. (See, e.g., Figs. 8-9, the gate dielectric layer 112 is over the doped regions 134.)

Claim Rejections - 35 USC § 102

As mentioned above, Applicants have amended Claim 14 by adding the limitation of "a second gate dielectric layer formed on said substrate covering said second channel and said second source/drain regions", which is believed to overcome the rejection under 35 U.S.C. §102(e) as being anticipated by US 6,635,505 of Tanaka et al.

The semiconductor device taught by Tanaka is different from the present invention. As shown in Figs. 12B-C of US 6,635,505, the gate insulating film (1122) does not cover the impurity region (1123). More specifically, referring to column 15, lines 3-6, Tanaka et al. teach removing the gate insulting film (1105) by dry etching, so that only the gate insulting film (1122) remains, and the impurity region (1123) is exposed. This may cause the impurity region (1123) to be contaminated during the following steps and result in instability of the electronic properties. Further, the step of dry etching will undercut the gate insulting film (122), which will influence the subsequent covering step of depositing the first interlayer insulating film (1124), so that a short circuit may occur between the drain/source wiring (1126/1127) and the gate wiring (1107).

In contrast, as recited in Claim 14 of the present application, the second source/drain regions are covered by the second gate dielectric layer. This characteristic has advantages of protecting the second source/drain regions from any contaminations during subsequent procedures, so that the resultant semiconductor device will have high performance in electricity

Serial No.: 10/690,703
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Inventor: SHIH-CHANG CHANG ET AL.

Attorney's Docket No.: LEE0023-US
Page 11

without losing uniformity. Tanaka et al. do not teach or suggest this advantageous feature.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejection.

In view of the foregoing, all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone Applicants' undersigned representative at the number listed below.

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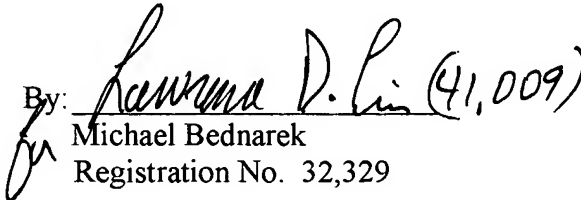
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Respectfully submitted,

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